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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,081	09/10/2003	Jigish D. Trivedi	MIO 0079 VA	2733

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EXAMINER	
FOURSON III, GEORGE R	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,081	TRIVEDI ET AL.	
	Examiner	Art Unit	
	George Fourson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-15,20,27-29 and 31-40* is/are allowed.

6)☒ Claim(s) *1,16-19,21-26 and 30* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/08.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim 21 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 21 does not further limit the subject matter of claim 1 because of the subjectivity associated with use of "ultra thin".

Claims 1,21,22,23,24,25 and 26 are rejected under 35 U.S.C. 1 03(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in combination with Kizilyalli et al.'807.

AAPA admits to a SRAM device with CMOS structure 4 substantially as claimed to have been known prior to applicant's invention with the exclusion of a diffusion barrier layer formed between a portion of polysilicon layer and metal, metal silicide or metal nitride film (Instant Page 4, Figs. I and 2, and page 8, line 12 to page 9, line 15).

Kizilyalli et al. discloses a semiconductor structure for a memory device such as SRAM which includes semiconductor substrate 16 (Col. 2, line 49, and Fig. 1), P-well 24 and N-well 26 in substrate 16 (Col. 2, lines 49-50), isolation region 28 that isolates active regions formed in respective P-well 24 and N-well 26 (Col. 2, lines 53-57), and polysilicide gate electrode structure composed of polycrystalline silicon film 20 by formation of N+ polysilicon layer 30 located above P-well 24 followed by formation of P+ polysilicon layer 32 located above n-well region 36 (Co1. 2, lines 57-60), diffusion barrier layer 50 formed over a portion of polysilicon film 20 wherein the portion includes N+ polysilicon layer 30 (Col. 2, line 60 to Col. 3, line 41 , and Col. 4, lines 11 -14) thereby blocking migration of P+ dopants through metal silicide film 60 over path 72 (Col. 4, lines 23-26 and lines 30-33) and blocking migration of N+ dopants through metal

silicide film 60 and P+ polysilicon layer 32 over path 88 (Col. 4, lines 34-37, and Fig. 5) and metal silicide film 60 formed over polysilicon film 20 (Col. 3, lines 66-67).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of the AAPA with Kizilyalli et al. because it would enable formation of diffusion barrier layer 50 of Kizilyalli et al. in AAPA'S CMOS structure 4 and obtain further advantage of minimizing dopant penetration and migration (Kizilyalli et al., Col. I , lines 53-55).
The choice of thickness of the polycrystalline silicon film would have been a matter of routine optimization to achieve the desired device density and the desired device characteristics of the device to be formed. (See MPEP 2 144.05).

The choice of thickness of the diffusion barrier layer and polysilicon layer would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

Claims 16,17,18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Kizilyalli et al. as applied to claims 1,21,22,23,24,25 and 26 above, and further in view of Fujii et al. '010.

The combination does not disclose forming an isolation region as recited.

Fujii et al. discloses a CMOS structure which includes P-type semiconductor substrate 1 (Col. 3, lines 52-53), N-well 2 formed in substrate 1 (Col. 4, lines 4-7), isolation region 3 (Col. 4, lines 7-8), active areas 4 and 5 formed in P-type region of substrate 1 and N-well 2 (Co1. 4, lines 9-13, and Fig. 2A), and polysilicide gate electrode structure composed of polysilicon layer 9 formed over gate oxide film 8 (Col. 4, lines 15- I 7), then first P+ doped region 9a is formed in a

portion polysilicon layer 9 (Co1. 4, lines 1 7-22), subsequently second N+ doped region 9b is formed in a second portion of polysilicon layer 9 (Col. 4, lines 23-28, and Fig. 2B), and metal silicide layer 12 over polysilicon layer 9 (Col. 4, lines 29-31 , and Fig. 2C).

In view of the disclosure of Kizilyalli et al. wherein diffusion barrier layer 50 is formed over first doped region 30 in polysilicon film 20 in order to prevent subsequent introduction of a second dopant to form second doped region 32 (Co1. 3, lines 55-65, and Fig. 3), it would have been within the scope to one ordinary skill in the art to combine the teachings of Fujii et al. with the combination because it would enable formation of an isolation region as is disclosed to useful by Fujii et al.

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Kizilyalli et al. and Fujii et al as applied to claims 16-19 above, and further in view of Hunter et al '725.

AAPA admits to a SRAM device with CMOS structure 4 substantially as claimed to have been known prior to applicant's invention with the exclusion of a nitride diffusion barrier layer formed between doped regions of the polysilicon layer and metal, metal silicide or metal nitride film (Instant Figs. 1 and 2, and page 8, line 12 to page 9, line 15).

Hunter et al. discloses a semiconductor structure in semiconductor devices for inhibiting out diffusion of dopants from a first conductive layer such as polycrystalline silicon to a second conductive layer such as silicide conductive material which includes a semiconductor substrate 36 and isolation region 34 (Co1. 3, lines 57-58, and Fig. 2A), N-well 38 and P-well 40 formed in substrate 36 (Col. 3, lines 61-62), polysilicide gate electrode structure composed of polysilicon film 44 comprised of N+ polysilicon layer 45 and P+ polysilicon layer 46 (Col. 4, lines 4-8),

sputter deposited nitride diffusion barrier layer 48 formed on surface of polysilicon layer 44 (i.e. N+ polysilicon layer 45 and P+ polysilicon layer 46) (Col. 4, lines 12-15, and Fig. 2C) and conductive layer 50 such as metal silicide (Col. 4, lines 57-59, and Fig. 2D).

It would have been within the scope to one ordinary skill in the art to combine the teachings of AAPA with Hunter et al. because it would enable formation of diffusion barrier layer 48 in AAPA'S CMOS structure 4 and obtain further advantage of inhibiting out diffusion of dopants from polycrystalline silicon into silicide conductive layers (Hunter et al., Col. 2, lines 64-67).

The choice of thickness of the polycrystalline silicon film would have been a matter of routine optimization to achieve the desired device density and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

The choice of thickness of the diffusion barrier layer would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

Claims 2-15,20,27-29 and 31-40 are allowed.

Claim 21 is objected to.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Fourson whose telephone number is (571)272-1860272-1860. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Fourson
Primary Examiner
Art Unit 2823

GFourson
March 22, 2005